Claims 29 and 40 have been amended with regard to the same mask used in the etching step. In claim 29, the same mask is formed on the third insulating film and the another part of the second insulating film, and in claim 40 the same mask is formed on the third insulating film and the second portion of the second insulating film. None of the applied prior art discloses such methods.

First, the Office Action correctly finds that there is no suggestion in Chow et al. of the removing step of claim 29. The Office Action looks to Mu et al. to cure this deficiency of Chow et al., referring to Figs. 2-8. These figures show opening 30 formed by coating photoresist on nitride layer 23, patterning the photoresist layer and etching the nitride and BPSG layers, as described in column 6, lines 8-15. Also, the channels in layer 8 Chow et al. are formed by patterning a photoresist layer formed on layer 8, as described in column 3, lines 31-32. It also not clear how the etching of Mu et al., where films 22 and 23 are etched, would be applied to Chow et al., as the film 6 already serves as the mask. There is no suggestion of a mask formed on a third insulating film and another part of a second insulating film exposed to the groove, as recited in claim 29, in either of Chow et al. or Mu et al.

Koerner et al. describes forming films of different materials with breaking vacuum, and Roth et al. is relied on for a carbon etch-stop layer. Even if such teachings could be combined with that of Chow et al. and Mu et al., the combination would still fail to suggest claim 29 since no reference, or the combination of references, suggests the a method where a step uses the recited mask. Allowance of claim 29 therefore respectfully requested.

Claim 40 is also in condition for allowance as none of the cited references, or a combination of the references, discloses a method having a step of forming a groove using a mask formed on the another portion of the second insulation film and the third insulation film. In Chow et al. a photoresist layer is formed on layer 8, and in Mu et al. a photoresist layer is formed on layer 22. Koerner et al. and Roth et al. are silent regarding the cited mask.

Claim 40 is also in condition for allowance, and allowance of claim 40 is respectfully requested.

Finally, the attention of the Patent Office is directed to the change of address of Applicants' representative, effective January 6, 2003:

Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

1940 Duke Street

Alexandria, VA 22314.

Please direct all future communications to this new address.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Respectfully submitted,

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Marked-Up Copy
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IN THE CLAIMS

Please amend the claims as follows:

29. (Four Times Amended) A process of fabricating a semiconductor device comprising the steps of:

forming a first insulating film on a semiconductor substrate;

forming a second insulating film on said first insulating film, said second insulating film being made of a material different from that of the first insulating film and having a thickness smaller than that of the first insulating film;

forming a third insulating film on said second insulating film, said third insulating film being made of a material different from that of the second insulating film having a thickness larger than that of the second insulating film;

forming a groove in a region of said third insulating film, in which a wiring is to be formed, said groove having a bottom to which said second insulating film is exposed;

removing a part of that portion of the second insulating film which is exposed to the groove, and a part of the first insulating film under the portion of the second insulating film, using the same etching mask formed on said third insulating film and on another part of said portion of the second insulating film which is exposed to the groove, and thus forming a contact hole reaching to the semiconductor substrate; and

burying the groove and the contact hole with copper to form a copper wiring in said groove and a copper contact in said contact hole, and controlling said burying with said copper to avoid formation of a native oxide.

40. (Twice Amended) A process of fabricating a semiconductor device comprising the steps of:

forming a first insulating film on a semiconductor substrate;

forming a second insulating film on said first insulating film, said second insulating film being made of a material different from that of the first insulating film and having a thickness smaller than that of the first insulating film;

forming a third insulating film on said second insulating film, said third insulating film being made of a material different from that of the second insulating film and having a thickness larger than that of the second insulating film;

forming a groove in said third insulating film having a bottom comprising said second insulating film; and

forming copper in said groove, wherein forming said copper is controlled to avoid formation of a native oxide;

wherein said step of forming said groove comprises[;], using the same mask:

etching through said second insulating [insulation] film to expose said first insulating [insulation] film while leaving a remaining second portion of said second insulating [insulation] film; and

removing a third portion of said first insulating [insulation] film to expose said substrate while leaving a remaining fourth portion of said first insulating [insulation] film, and

wherein said mask is formed on third insulating film said second portion of said second insulating film.